**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Applicant: | Efland | Docket No: | TI-30955 |
| Serial No: | 10/039,663 | Examiner: | Adujar, L. |
| Filed: | 10/22/2001 | Art Unit: | 2826 |

For: INDIVIDUALIZED LOW PARASITIC POWER DISTRIBUTION LINES DEPOSITED OVER ACTIVE INTEGRATED CIRCUITS

## APPEAL BRIEF PURSUANT TO 1.192(c)

**MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)**
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on 5-21-04.

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed October 8, 2003, and the Advisory Action mailed February 18, 2004.

## REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

## RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected or have a bearing on the Board's decision.

## STATUS OF THE CLAIMS

Claims 1-28 were originally filed and Claims 6, 10, 12, and 24-28 have been cancelled and Claims 29-34 have been added.

## STATUS OF AMENDMENTS

The application was originally filed with Claim 1-28. By virtue of an amendment filed on April 15, 2003, Claims 6, 10, 12, and 24-28 were cancelled and Claims 29-34 were added. A Response After Final was filed on December 23, 2003, amending no claims.

## SUMMARY OF THE INVENTION

FIG. 1 shows a portion of an IC chip 110, which has a first ("active") surface 110a and a second ("passive") surface 110b. The second chip surface 110b is mechanically attached by adhesive material 140 to the chip mount pad 151 of a pre-fabricated metallic leadframe 150. Leadframe 150 further has a plurality of segments 152, which serve as electrical leads to outside parts.

As an example, the IC 130 comprises a plurality of lateral DMOS transistors fabricated in p-epitaxial layer 121.

Subsequently to the steps necessary to fabricate elements of lateral DMOS transistors into surface 110a, a multilevel interconnection hierarchy is constructed on top of surface 110a. The construction starts with the deposition of an interlevel insulator layer 131. Insulator layer 131 is then patterned and etched to form vias 132, using standard photolithographic techniques. Metallization layer 133 is deposited over insulator layer 131 and into vias 132 and patterned and etched. Metal layer 133 is sometimes referred to as "metal 1".

A second interlevel insulator layer 134 is then deposited over metallization layer 133 and patterned and etched to form vias 135 therein. Next, metallization layer 136 is deposited over insulator layer 134 and into vias 135 and patterned and etched. Metal layer 136 is sometimes referred to as "metal 2".

Next, a protective overcoat layer 111 is deposited on the surface of the semiconductor wafer, uniformly covering the last metallization layer 139.

Using standard photolithographic techniques, vias 161 are formed through the overcoat layer (or layers) 111 to expose the metallization layer intended for serving power current or electrical ground potential in the IC.

The next process steps comprise the deposition and patterning of power distribution lines 160. Metals, thicknesses and widths of lines 160 are configured such that the electrical resistance for any current will be small; a preferred design goal is a sheet resistance of less than 1.5 mΩ/□, typically 1.3 mΩ/□.

Via 161 is filled with the first metal layer 162 of the layers forming stack 160. Stack 160 consists of a seed metal layer 162, a first stress-absorbing metal layer 163, a second stress absorbing layer 164 and an outermost bondable (and/or solderable) metal layer 165. The seed metal layer is electrically conductive, provides adhesion to both the metal 139 and the protective overcoat, permits the exposed portions of its upper surface to be electroplated, and prevents migration of the subsequent stress-absorbing metals to the bus metallization layers.

The outermost layer 165 is metallurgically bondable and/or solderable.

The plating pattern of the power distribution lines may form any desired layout (as illustrated, for example, in FIG. 7). The preferred pattern, however, is to have the majority of lines formed as straight lines between vias such as via 161 in FIG. 1 and the

conductor 170 connecting to leadframe segments 152, thereby minimizing the distance and thus the electrical resistance between a selected segment 152 and a corresponding active IC component, to which power has to be delivered.

In FIG. 3 (known technology), the bond pads are aligned close to the chip periphery, more or less in linear arrays around the central active IC area.

In FIG. 4 (this invention), all bond pads are placed over active IC area. As a consequence of this arrangement, a substantial amount of silicon real estate is saved. In addition, a number of contact pads, which supply power current to the active IC, are combined into several power distribution lines (marked by different shading in FIG. 4). These lines are preferably patterned as approximately straight lines, but may have variable widths at various locations.

FIG. 4 illustrates an additional electrical advantage of the present invention. The network of the power distribution lines can be patterned so that parasitic inductances between the network lines are minimized.

A significant electrical advantage of the present invention is indicated by the comparison of FIGs. 5A and 5B.

FIG. 5B depicts the two pads 503 and 504 arranged in positions over the active IC area according to the present invention.

FIG. 5B indicates schematically the electrical advantages for the supply of power current provided by the positioning of the wire bonds over the active IC area, especially when patterned into a power distribution line.

FIG. 6 is a schematic top view of an IC chip summarizing a general plan for geometrical layout of power distribution lines deposited over the active IC, and for the electrical features as far as they relate to lowering the electrical parasitics.

## ISSUES

The six issues on appeal are first whether Claim 2 is unpatentable under 35 U.S.C. § 112, second paragraph; second whether Claim 1 is being anticipated by Yamasaki; third whether Claims 2 and 3 are unpatentable over Yamasaki; fourth whether Claims 4, 5, 7, 8, 11, 15, 20, 21, and 23 are unpatentable over Yamasaki in view of Tani; fifth whether Claim 9 is unpatentable over Yamasaki in view of Tani and in view of alleged admitted prior art; and sixth whether Claims 13, 20, and 22 are unpatentable over Yamasaki in view of Tani and Wolf..

## GROUPING OF THE CLAIMS

Each of Claims 1, 2, and 4 as contained in the attached Appendix are independently patentable and these claims do not stand or fall together for the reasons more clearly set forth herein below.

## ARGUMENTS

Claim 2 is in full compliance with 35 U.S.C. § 112, second paragraph. The Examiner alleges that the symbol "□" is not based on any standard. The units of the claims resistance are milliohms per square which is well known in the industry as a measure of sheet resistance.

Furthermore, it does not matter whether or not the "□" corresponds to any standard but whether or not the claims set forth and defines a particular area for which the Appellant wishes patent coverage. In this connection since of the well known meaning of "□", it is respectfully submitted that Claim 2 set forth a particular area for which patent protection is sought.

Claim 2 particularly points out and distinctly claims the subject matter which Applicants believe is their invention.

It is respectfully submitted that Yamasaki does not disclose or suggest the presently claimed invention including the network of power distribution lines deposit on the surface of the chip over active components of the circuit as defined in independent Claim 1, albeit defined as electrically conductive films pattern into a network of lines substantially vertically over the active components in independent Claim 4.

The Examiner alleges that Yamasaki discloses in element 70 an active component.

However, the Examiner's attention is directed to column 2, lines 53-55 were Yamasaki discloses that element 70 is a noise removing capacitor.

Capacitors are passive elements.

Tani does not disclose or suggest the presently claimed invention including the network or power distribution lines deposit on the surface of the chip over active components of the circuit as defined in the various forms in independent Claims 1 and 4.

There is nothing in Tani to suggest this feature.

Whether or not the alleged admitted prior art discloses that it is common practice to manufacture single piece lead frames from a thin sheet of metal or whether one of ordinary skill in the art would consider modifying either Yamasaki or Tani is of no moment since the result in construction would still in no way disclose or suggest the presently claimed invention.

Wolf does not cure the above noted defects.

## CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-5, 7-9, 13, 15, and 20-23 under 35 U.S.C. § 112 and 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

W. Daniel Swayze, Jr.
Attorney for Appellants
Reg. No. 34,478

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5633

## APPENDIX

Claim 1 (original): An integrated circuit chip mounted on a leadframe, said leadframe having a plurality of segments, comprising:

a network of power distribution lines deposited on the surface of said chip over active components of said circuit;

said lines connected vertically to said components by metal-filled vias, and also to said segments by conductors; and

the majority of said lines patterned as straight lines between said vias and said conductors, respectively, thereby minimizing the distance for power delivery between a selected segment and one or more corresponding active components, to which said power is to be delivered.

Claim 2 (original): The chip according to Claim 1 further having said lines fabricated with a sheet resistance of less than 1.5 mΩ/□ and positioned to minimize parasitic electrical losses in power delivery between a selected segment and one or more corresponding active components, to which said power is to be delivered.

Claim 3 (original): The chip according to Claim 2 wherein said parasitic electrical losses include voltage drops during said power current flow, capacitances between said network and said active components, and inductances between network lines.

Claim 4 (previously presented): A semiconductor device wherein electrical parasitics are minimized by individualized power distributors deposited over active integrated circuit components, comprising:

a semiconductor chip having first and second surfaces;

an integrated circuit fabricated on said first chip surface, said circuit having active components, contact pads, at least one metal layer, and being protected by a mechanically strong, electrically insulating overcoat having a plurality of metal-filled vias to contact said at least one metal layer;

electrically conductive films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components, said films in contact with said vias and having an outermost film of non-corrodible, metallurgically attachable metal;

said network patterned to distribute power current while minimizing parasitic electrical losses between said network and said active components;

said network further patterned to minimize silicon real estate consumed by power interconnections between said active components;

a leadframe having a chip mount pad, a first plurality of segments providing electrical signals, and a second plurality of segments providing electrical power and ground;

said second chip surface attached to said chip mount pad;

electrical conductors connecting said contact pads with said first plurality of segments; and

electrical conductors connecting said network lines with said second plurality of segments.

Claim 5 (original): The device according to Claim 4 wherein said chip is selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material customarily used in electronic device fabrication.

Claim 6 (cancelled).

Claim 7 (original): The device according to Claim 4 wherein said integrated circuit comprises multi-layer metallization, at least one of said layers made of pure or alloyed copper, aluminum, nickel, or refractory metals.

Claim 8 (original): The device according to Claim 4 wherein said overcoat comprises materials selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbon alloys, polyimide, and sandwiched films thereof.

Claim 9 (original): The device according to Claim 4 wherein said leadframe is pre-fabricated from a sheet-like material selected from a group consisting of copper, copper alloy, aluminum, iron-nickel alloy, or invar.

Claim 10 (cancelled).

Claim 11 (original): The device according to Claim 10 wherein said encapsulation comprises a polymer compound fabricated in a transfer molding process.

Claim 12 (cancelled).

Claim 13 (original): The device according to Claim 4 wherein said lines and contact pads are attached to outside parts by solder balls.

Claim 14 (original): The device according to Claim 4 wherein said conductive films comprise a stack of stress-absorbing metal films under said outermost metallurgically attachable film.

Claim 15 (previously presented): The device according to Claim 4 wherein said electrical conductors are selected from a group comprising wire ball and stitch bonding, ribbon bonding, and soldering.

Claim 16 (original): The device according to Claim 14 wherein said stack of films comprise a layer of seed metal, promoting adhesion to said vias and inhibiting migration of overlying metals to said vias, at least one stress- absorbing metal layer, and an outermost metallurgically attachable metal layer.

Claim 17 (original): The device according to Claim 16 wherein said seed metal is selected from a group consisting of tungsten, titanium, titanium nitride, molybdenum, chromium, and alloys thereof.

Claim 18 (original): The device according to Claim 16 wherein said stress-absorbing metal layer comprises at least one layer selected from a group consisting of copper, nickel, aluminum, and alloys thereof.

Claim 19 (original): The device according to Claim 16 wherein said outermost metal layer is selected from a group consisting of pure or alloyed aluminum, gold, palladium, silver and platinum.

Claim 20 (original): The device according to Claim 4 wherein said conductors are bonding wires, bonding ribbons, or solder balls.

Claim 21 (original): The device according to Claim 20 wherein said bonding wire is selected from a group consisting of pure or alloyed gold, copper, and aluminum.

Claim 22 (original): The device according to Claim 20 wherein said solder ball is selected from a group consisting of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.

Claim 23 (original): The device according to Claim 4 wherein said network of lines is electrically further connected to selected segments suitable for outside electrical contact.

Claims 24-28 (cancelled).

Claim 29 (previously presented): An integrated circuit chip mounted on a leadframe, said leadframe having a plurality of segments, comprising:

a network of power distribution lines deposited on the surface of said chip over active components of said circuit;

said lines comprising a stack including a stress-absorbing metal film;

said lines connected vertically to said components by metal-filled vias, and also to said segments by conductors; and

the majority of said lines patterned as straight lines between said vias and said conductors.

Claim 30 (previously presented): The device of Claim 29, wherein said stack including a stress-absorbing metal film comprises an outermost metallurgically attachable film.

Claim 31 (previously presented): The device of Claim 29, wherein said stack including a stress-absorbing metal film comprises a layer of seed metal, a stress-absorbing metal layer on said seed metal layer, and an outermost metallurgically attachable metal layer.

Claim 32 (previously presented): The device of Claim 31, wherein said stress-absorbing metal layer comprises at least one layer selected from a group consisting of copper, nickel, aluminum, and alloys thereof.

Claim 33 (previously presented): The device of Claim 31, wherein said seed metal is selected from a group consisting of tungsten, titanium, titanium nitride, molybdenum, chromium, and alloys thereof.

Claim 34 (previously presented): The device according to Claim 31, wherein said outermost metal layer is selected from a group consisting of pure or alloyed aluminum, gold, palladium, silver and platinum.